

Battery charger indicates rate of charge

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A single LED indicates whether the battery charger in Fig 1 is delivering a trickle charge or a fast charge. During fast charges, the LED stays lit continuously because IC₂'s FASTCH output sinks dc. During trickle charges, the LED flashes because D₁ and Q₁ enable the 555 timer. The timer is an astable multivibrator operating at 60 Hz ($f=1/1.4RC$).

The timer remains enabled during a fast charge, but it must shut off upon disconnection of the battery. Zener diode D₁ makes that decision. With no battery connected (a condition that R₅ and an internal comparator sense), IC₂ produces a voltage at BATT+ equal to twice the number of cells for which the IC is programmed. This voltage (4V for two cells) turns on the 3.3V zener diode and disables the timer.

Connecting a battery drops the BATT+ voltage to 2.8V (1.4V per cell), thereby turning off D₁ and Q₁, and enables the timer. The timer's output drives Q₃, whose collector (in a wired-OR connection with the open-drain FASTCH output) causes the LED to flash. Other cell counts require different zener voltages (Table 1).

During a fast charge, the LED should glow steadily, without flicker that would occur if the timer were operating. This continuous-glow condition is assured if the FASTCH voltage remains low: IC₂'s data sheet guarantees 0.4V max when

TABLE 1—ZENER-DIODE VOLTAGE VS CELL COUNT

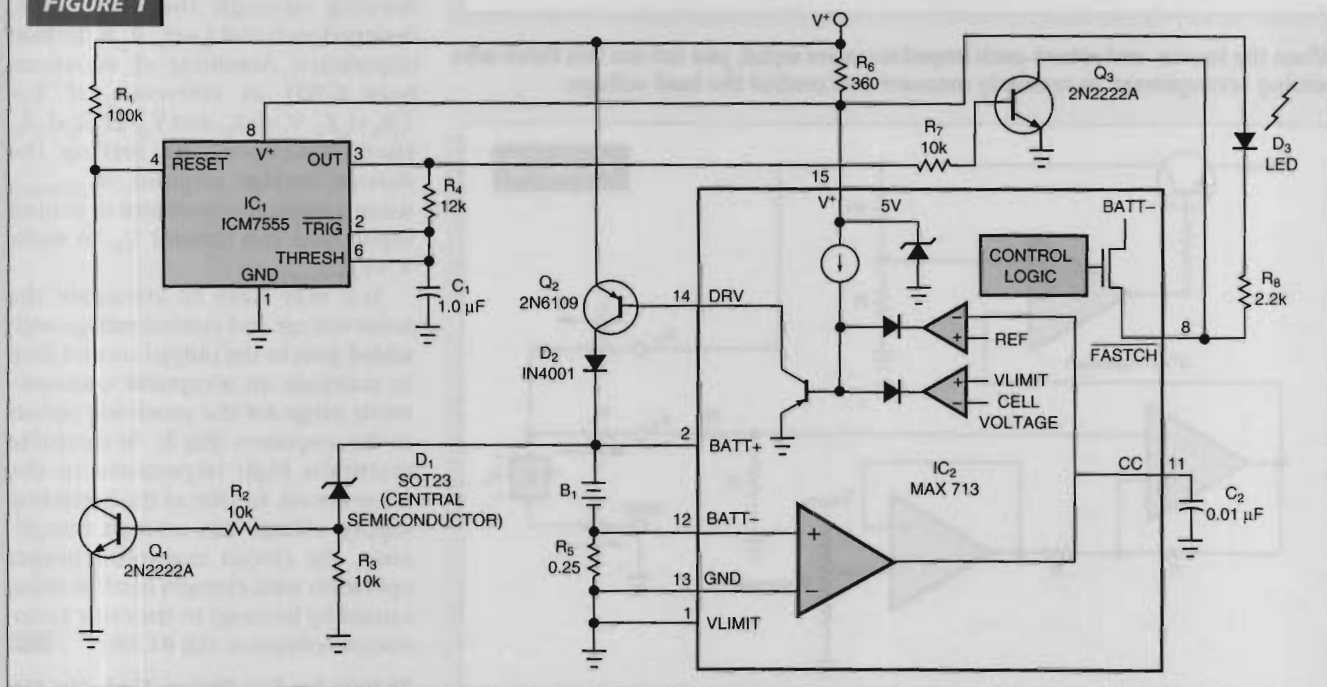
Cell count	BATT+ voltage (V)	Charged-battery voltage (V)	Required zener voltage (V)
2	4	2.8	3.3
4	8	5.6	6.8
6	12	8.4	10
8	16	11.2	15
10	20	14	18
12	24	16.8	18
14	28	19.6	24

FASTCH sinks 2 mA. Higher currents produce a higher voltage, which may result in flicker. In that case, you can cure the problem by adding a resistor in the emitter of Q₃. (DI #1705)

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FIGURE 1



The shaded components in this charger for NiCd or nickel-metal-hydride batteries cause the LED to flash during trickle charges and to glow continuously during fast charges.

Remote charging circuit uses three-wire sensing

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Remote voltage sensing usually uses a four-wire sensing system, which involves two conductors for high load-current flow and two high-impedance paths for accurately measuring

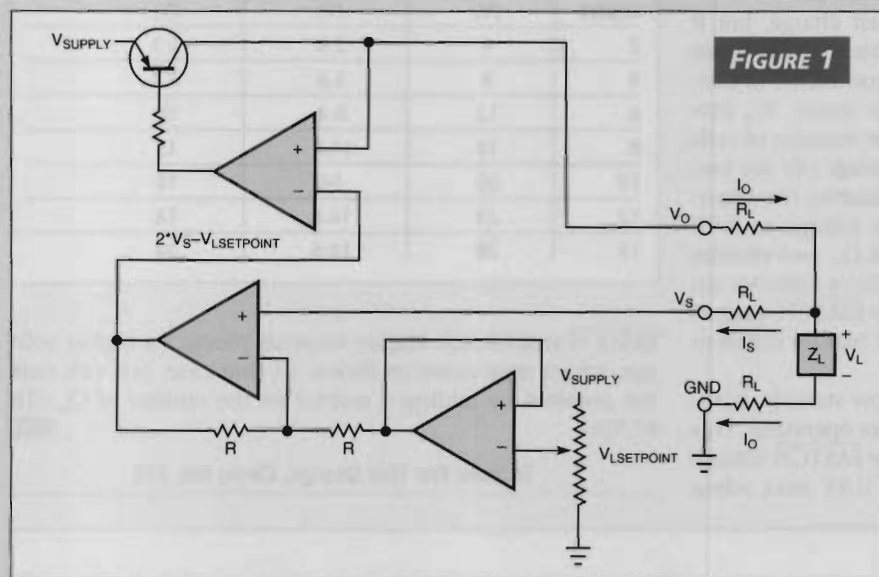
the remote voltage without incurring substantial ohmic losses. Voltage control at the load, therefore, entails measuring the "sense" pair and driving the "output" pair. Over cables in which the impedances in the source and return paths to the load are equal, you can use a three-wire sense system, thereby saving a conductor.

The circuit in Fig 1 takes advantage of equal resistance in the source and return paths. It uses a simple network to sense the remote voltage and drive the output to precisely control the remote voltage. In the output network, R_L represents the resistance of a single cable conductor, for example, 4Ω for 100 ft of #26 wire. V_O is the output voltage to the cable, with reference to the return lead (GND). V_S is the voltage of the sense lead, with reference to the return lead (GND). V_L is the desired voltage at the load, and I_O is the current flowing through the cable and load. I_S is the current flowing through the sense lead, designed such that $I_S \ll I_O$. Z_L is the load impedance. Assuming all equations have GND as reference, if $V_S = I_O R_L + I_O Z_L$, $V_L = I_O Z_L$, and $V_O = 2I_O R_L + I_O Z_L$, then $V_O = 2V_S - V_L$. By setting the desired voltage setpoint, $V_{LSETPOINT}$, using a manual adjustment or control input, you can control V_O to make $V_L = V_{LSETPOINT}$.

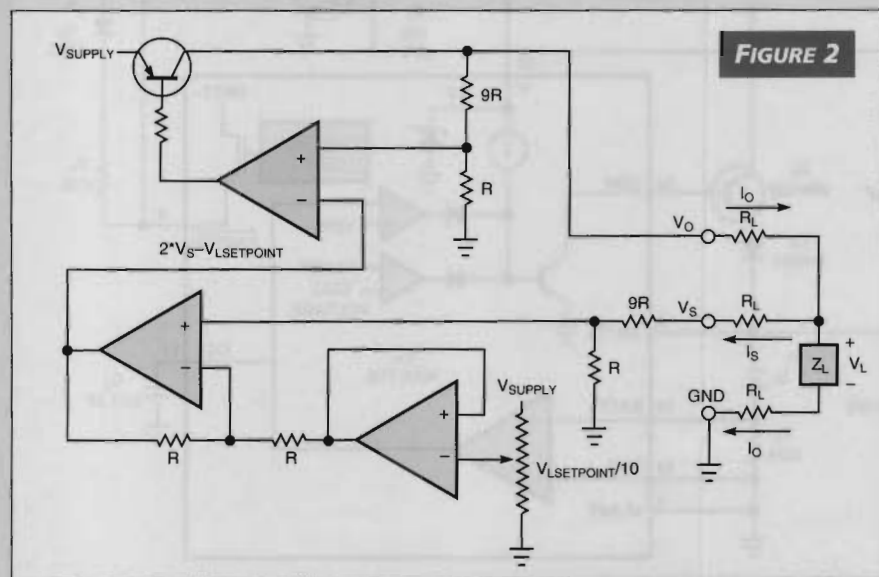
You may have to attenuate the sense voltage and control voltage with added gain in the output control loop to maintain an acceptable common-mode range for the processed signals in the amplifiers (Fig 2). Be careful to maintain high impedance in the sense circuit. Insofar as the regulating supply voltage has enough compliance, the circuit maintains proper operation with changes (such as those caused by heating) in the cable's conductor resistance. (DI #1706)

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When the source- and return-path impedances are equal, you can use this three-wire sensing arrangement to remotely measure and control the load voltage.



Adding attenuation and gain to the circuit in Fig 1 maintains acceptable common-mode range in the processed signals in the amplifiers.

Analog switch cuts peak-detector reset time

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The schematic in Fig 1 is a basic configuration for a unity-gain peak detector using the PKD-01FP monolithic peak detector from Analog Devices. The reset time, t_{RES} , is the time necessary to discharge the hold capacitor C_H . t_{RES} and the acquisition time t_{ACQ} are functions of the IC's output-current capability. With $C_H=10$ nF, this output-current limitation sets both t_{RES} and t_{ACQ} to about 220 μ sec.

You can obtain fast resetting, independent of the IC's output capability, by adding an analog switch in parallel with the hold capacitor (Fig 2). The p-channel JFET, Q_1 , buffers reset pulse V_{RES} to provide the needed V_{GS} drive level to the n-channel JFET, Q_2 . Pullup resistor R_1 guarantees an off condition for Q_1 ($V_{GS(OFF)}=4V$ max) with a high output in the CMOS logic block. When Q_2 turns on and discharges C_H , the discharge time constant is $t_{DIS}=C_H \cdot r_{DS(ON)}=600$ nsec, assuming a maximum value of 60 Ω for Q_2 's on-resistance at 25°C. Assuming a minimum reset-pulse duration of about five

times the discharge time constant, the reset time is 3 μ sec.

When Q_2 turns off, the drain cutoff current, $I_{D(OFF)}$, introduces a droop rate given by assuming a conservative maximum value of 250 pA for $I_{D(OFF)}$.

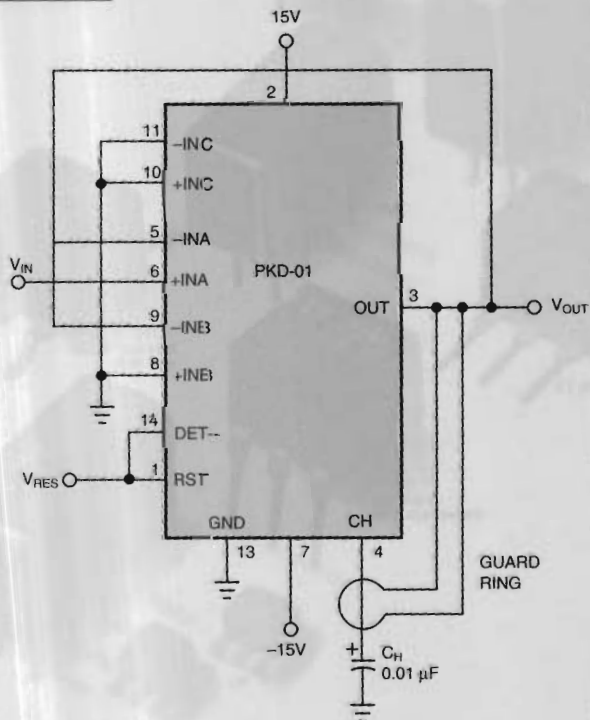
$$\frac{dV_{CH}}{dt} = \frac{I_{D(OFF)}}{C_H} = \frac{250 \text{ pA}}{10 \text{ nF}} = 25 \text{ } \mu\text{V/msec},$$

Q_2 introduces this additional droop rate, which is about one-eighth of the droop rate stemming from the PKD-01FP peak-detector IC. The use of a 2N4392 n-channel JFET for Q_2 , whose $I_{D(OFF)}=100$ pA, reduces the additional droop rate to one-twentieth the PKD-01FP contribution. (DI #1708)

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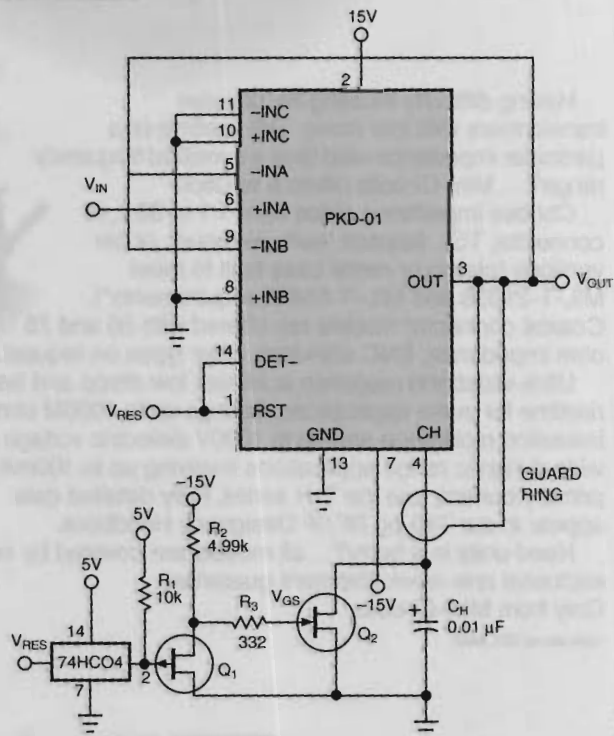
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FIGURE 1



In this unity-gain, peak-detector configuration, the discharge current available to the hold capacitor sets the reset time to about 220 μ sec.

FIGURE 2



The JFET analog switch, Q_2 , rapidly discharges the hold capacitor and thus lowers the reset time to about 3 μ sec.

IC forms differential line driver/receiver

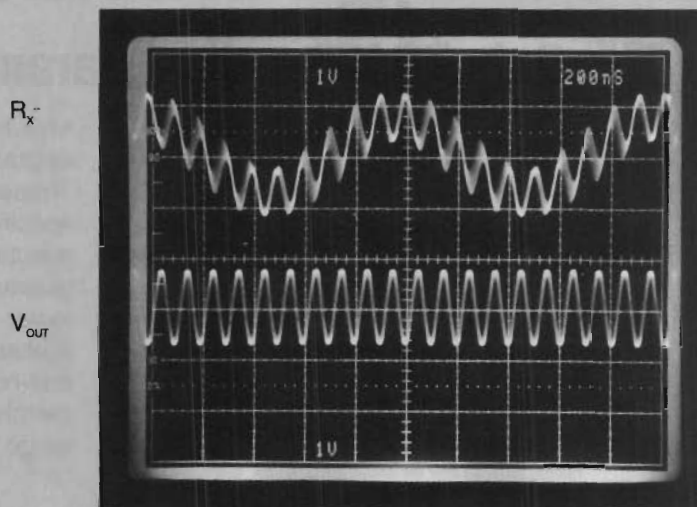
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You can use the HFA1212 dual video buffer to implement differential line drivers and receivers (Fig 1) with a minimum of external components. Common-mode rejection is a function of the internal matched thin-film resistors, which you can pin-strap to set the required loop gains. V_{IN} terminates in 75Ω and drives both amplifiers in IC₁. IC_{1A} and IC_{1B} have gains of -1 and +1, respectively. These amplifiers create a differential signal with a net gain of two. The 75Ω series resistors at the outputs provide impedance matching to the transmission line.

The 150Ω resistor on the receiver side of the transmission line provides proper impedance matching and attenuation for a gain of one at the receiver input. IC₂ performs differential-to-single-ended conversion and provides common-mode rejection. IC_{2A} is configured for a gain of +2. IC_{2B} subtracts common-mode signals and provides a gain of +2 to differential signals. When V_{OUT} terminates in 75Ω , the overall gain from V_{IN} to V_{OUT} is unity. Because of the gain of +2 in IC_{2A}, the peak voltage at the receiver may not exceed 1.5V.

The oscilloscope photo in Fig 2 shows the common-mode rejection of the receiver. V_{IN} is a 10-MHz, 1.5V p-p sine wave. A 1-MHz, 1.5V p-p common-mode signal drives the ground reference of Fig 1's IC₁ (with respect to the ground of IC₂). The upper trace shows the combined signal that appears at R_X . V_{OUT} , seen in the bottom trace, is a faithful reproduction of V_{IN} , with the com-

FIGURE 2



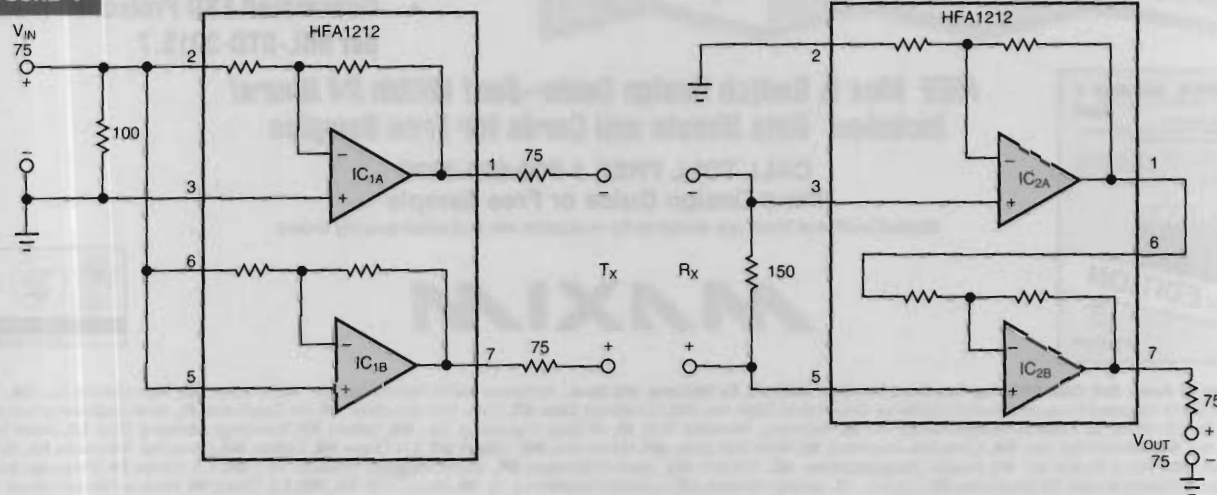
The receiver circuit of Fig 1 subtracts the 1-MHz common-mode signal in the top trace, to provide a faithful reproduction of the 10-MHz input signal.

mon-mode signal removed. (DI #1709)

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FIGURE 1



A dual video-buffer IC and a few resistors form a differential video line driver or receiver with a high common-mode rejection ratio. The external resistors provide impedance matching for the 75Ω transmission line.

Universal compensator neutralizes temperature coefficient

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The universal thermal-compensation module in Fig 1 can neutralize the temperature coefficient of both signs within a $\pm 0.6\%/^{\circ}\text{C}$ range. The circuit can compensate the temperature coefficient of offset voltage, gain, sensitivity, or, in general, the linear terms of a device's overall temperature behavior. The circuit consists of a pair of negative-temperature-coefficient (NTC) thermistors, labeled R_T , and of fixed resistors with calculated values that reduce the inherent nonlinearity of the thermistors. Because of this linearization, the overall nonlinearity stays within $\pm 1.2\%$ for a 0 to 50°C temperature range.

When the 1-M Ω potentiometer is in the maximum left position, the TC has a maximum positive value of $0.6\%/^{\circ}\text{C}$. In the maximum right position, the circuit produces maximum NTC of the same absolute value. You can continuously adjust the TC between these two extremes. For proper operation, good thermal contact is necessary between the module (the thermistors, primarily) and the device that you're compensating. The TC of the circuit depends only on the wiper position—not on the input voltage. So, you can adjust the output voltage and TC independently. The module has a gain of 0.5 at 25°C .

The resistor values in Fig 1 are the exact calculated numbers that provide the best linearization. These values are feasible in film technology with laser trimming. For discrete components, you simply have to choose the closest values. The circuit uses inexpensive, chip-NTC thermistors with nominal values of 1k at 25°C and constant $B=3100$, but any other types are applicable. However, differences in constant B may cause slightly higher nonlinearity. The power consumption of a thermistor is $\leq 0.1 \times V_{IN}^2$ mW. This power has to be small enough to avoid the self-heating of the thermistor body. In most practical cases, V_{IN} varies from 1 to 10V, so the power varies from 0.1 to 10 mW.

Performing the compensation requires that you first measure the output of the device at room temperature with the wiper electrode close to the center. Then, heat or cool the device to either a minus or plus temperature close to the margins, such as 0 and 50°C . Make the TC adjustment by rotating the wiper so that the error decreases. The criterion of

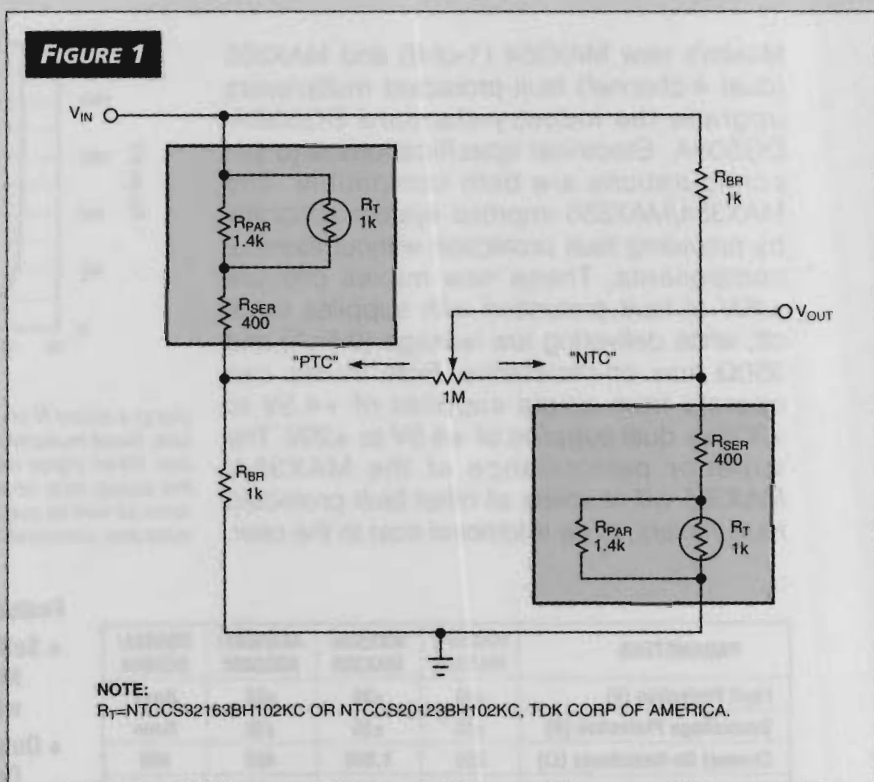


Fig 1—This thermal-compensation module reduces an external circuit's temperature coefficient to within $\pm 0.6\%/^{\circ}\text{C}$ range.

compensation is simple: The output of the device at temperature extremes should be the same as the room-temperature output.

Strictly speaking, this module can compensate only the linear part of the initial TC of a device. Residual TC of the device is 90% less than initial. The circuit can actually operate over a -25 to $+85^{\circ}\text{C}$ temperature range, but was optimized for a 0 to 50°C operating range. You may see increasing nonlinearity outside of this range. A special program can estimate the nonlinearity in any temperature range and can calculate the proper values of the resistors. (The program is available from the author.)

For precise compensation, a reduced range of TC is preferable. Choosing $R_{PAR}=800\Omega$, $R_{SER}=2.5\text{ k}\Omega$, and $R_{BR}=3\text{ k}\Omega$ reduces the full range of TC to $\pm 0.1\%/^{\circ}\text{C}$. (DI #1703)

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Universal watchdog fully controls μ P reset

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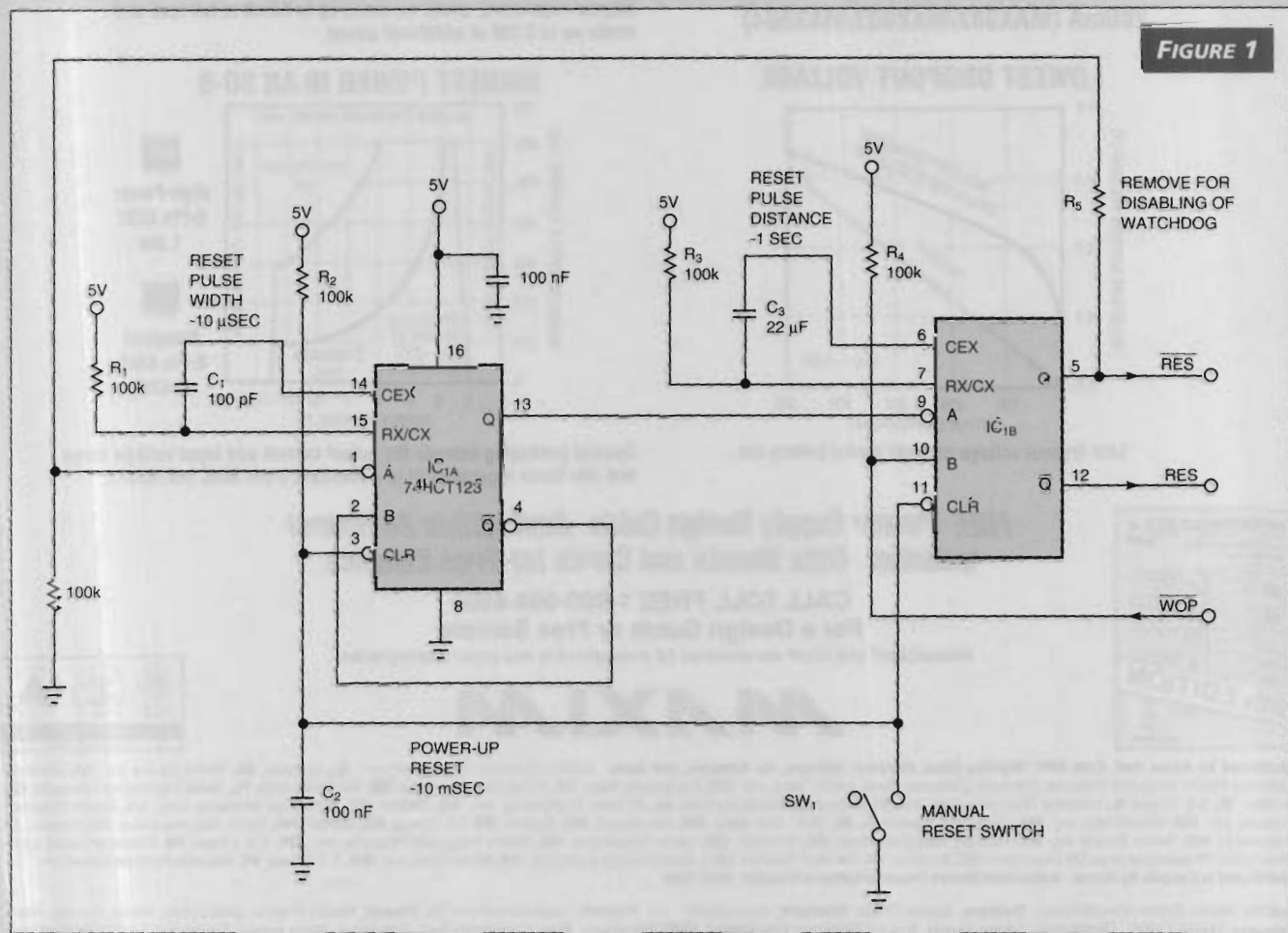
Many μ Ps contain internal watchdog timers, and you may wonder why you need another stand-alone circuit. Unfortunately, more highly integrated functions have preset parameters that you may want to change. Also, internal watchdogs are generally a simple combination of a flip-flop and a timer. If the program does not start properly on the first try, the timer is of no use because the program never turns on the watchdog. This watchdog catches *exactly* this condition.

The design in **Fig 1** allows you to set all parameters and fully control the reset of the μP . The circuit consists of two serially coupled one-shots in IC_{1A} . IC_{1A} controls the reset pulse width using R_1 and C_1 , and IC_{1B} controls the distance between pulses using R_3 and C_3 . The μP should apply a short negative pulse to the watchdog input at R_4 . If this signal is static long enough and enables IC_{1B} to time out, the circuit

returns a reset pulse. At power-up, the circuit activates reset for a longer time using R_2 and C_2 , enabling the processor clock to stabilize. Pushing SW_1 performs a manual reset. You can also disable the watchdog function by removing R_5 if special testing is necessary, such as when you implement the WDPulse for the first time. In this mode, IC_{1A} retriggers itself, disabling IC_{1B} .

This design uses cheap, off-the-shelf components, is flexible, is reliable, and has moderate power consumption of approximately <2 mA. The one thing missing is a supply-voltage monitor. You can add one using an ordinary op amp or a simple IC, such as the MAX809. You can simply insert this IC between 5V and R₁. (DI #1704) 

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**FIGURE 1**

This universal watchdog timer allows you to set all parameters and fully control a μ P's reset.